T 52: Silicon Detectors V

Time: Wednesday 16:15–18:15 Location: KH 01.012

T 52.1 Wed 16:15 KH 01.012

Performance of FBK Trench-Isolated LGAD coupled to Timpix3 Chip — •Chin-Chia Kuo, Erika Garutti, Jörn Schwandt, Annika Vauth, and Constanze Wais — University of Hamburg, 22761, Luruper Chaussee 149, Hamburg, Germany

The widely used instrumentation telescope operated at the DESY-II beam lines consists of six sensor planes using MIMOSA 26 monolithic active pixel devices for track reconstruction. However, the readout time of the current telescope is around 115 μs. As a result, a time reference layer is necessary to properly associate telescope tracks with the hits in the device under test. Additionally, a layer with high time resolution would provide a reference for the characterization of timing detectors. The low-gain avalanche diode (LGAD) with a good time resolution at the picosecond level is a good candidate for this purpose. LGAD with an isolated trench design is chosen for the study. With the trench design, the multiplication layer is extended, resulting in a better fill factor. In this presentation, the performance of FBK TI-LGAD bump-bonded to the Timepix3 chip is presented, including the gain factor, efficiency, and time resolution. Modules are tested at the DESY testbeam facility, using electrons with an energy of 3 GeV.

T 52.2 Wed 16:30 KH 01.012

Characterization of CASSIA 1, an LGAD design in a commercial CMOS imaging process — •Silas Müller, Christian Bespin, Hans Krüger, Lars Schall, Sinou Zhang, Alexander Walsemann, Rasmus Partzsch, Fabian Hügging, and Jochen Dingfelder — Physikalisches Institut der Universität Bonn, Nußallee 12, 53115 Bonn

Next-generation detector technologies have to cope with high rate environments, where precise time-tagging is needed. Sensors with internal gain may offer several advantages for these applications. They can achieve higher signal amplitudes, which can simplify the design of in-pixel electronics, and their superior timing performance may be beneficial for future 4D tracking or time-tagging applications. The CASSIA project (CMOS Active SenSor with Internal Amplification) seeks to develop monolithic active pixel sensors (MAPS) with internal signal gain and low noise, implemented within the Tower Semiconductor 180 nm process. This talk presents first characterization results from CASSIA 1, a prototype designed to test the feasibility of integrating a gain layer in a 180 nm commercial CMOS imaging Tower Semiconductor process. Different gain layer configurations are examined and results from electrical tests as well as measurements with radioactive sources are shown. Gain measurements obtained with pulsed lasers of different wavelength and initial test beam results are presented.

T 52.3 Wed 16:45 KH 01.012

Test beam studies of Resistive Silicon Detectors — •Niyathikrishna Meenamthuruthil Radhakrishnan[3], Roberta Arcidiacono[1], Nicolo Cartiglia[2], Alexander Dierlamm[3], Ling Leander Grimm[3], Lorena Hahn[3], Markus Klute[3], Aurora Losana[4], Brendan Regnery[3], and Luca Menzio[5] — [1]Univesita di Piemonte Orientale — [2]Istituto Nazionale di Fisica Nucleare — [3]Karlsruhe Institute of Technology, Karlsruhe, Germany — [4]University of Turin — [5]CERN

Resistive Silicon Detectors (RSDs) are among the most promising candidates for 4D tracking for future colliders where precise position and timing information will be quintessential for tracking. RSDs are based on the Low Gain Avalanche Diode technology with an additional resistive layer which enables spread of signal so that a single particle hit induces signal on multiple readout pads, and the reconstruction results in a higher resolution compared to traditional pixelated or strip detectors. The talk will give a summary of the results obtained from the data collected during the test beam measurements at the H6B beam line of the CERN SPS North Area with 120 GeV pions in October 2025. The setup consisted of two DC coupled RSD sensors and one AC coupled RSD sensor. This talk will emphasize the efforts to improve track reconstruction and analysis of test beam data with the software framework, Corryvreckan.

T 52.4 Wed 17:00 KH 01.012

A novel Low Gain Avalanche Diode design: MARTHA — •E. C. Wais[1], A. Baehr[2], J. Damore[2], E. Garutti[1], C. Koffmane[2], J. Ninkovic[2], E. Prinker[2], R. H. Richter[2], G. Schaller[2], F. Schopper[2], J. Schwandt[1], and J. Tries[2] — [1]University of Hamburg — [2]Semiconductor Laboratory of the MPG

To cope with the high interaction rates of new colliders, detectors with time resolution in the range of 10 ps are required to disentangle pile-ups. LGADs are a promising candidate for this task. LGADs feature a low amplification gain, which enables good timing resolution in thin sensors. However, due to the strong electrical field in the gain region, LGADs tend to break down at the pixel edges. In order to overcome this, the sensors have to be equipped with complex separation structures, which usually result in dead areas without gain between pixels. The Monolithic Array of Reach THrough Avalanche diodes design aims to tackle this problem, by combining a deeply implanted gain layer followed by an additional n-doped Field Drop Layer. This reduces the electric field at the n+-edges, thereby preventing them from breaking down. Since the gain region is not segmented, there are no dead spaces in the inter-pixel regions. A first prototype batch with test structures is being investigated. The sensors are optimized for photon detection without any specific timing requirements and are expected to have a fill factor of 100%. Future R&D aims to optimize this design for fast timing applications. In this talk, the MARTHA concept, characterization measurements and first test beam data from the DESY 2 test beam facility, are presented.

T 52.5 Wed 17:15 KH 01.012

Probing the Acceptor Removal Effect in Silicon Test Diodes Mimicking LGAD Gain Layers — •P. Erberk, E. Garutti, J. Schwandt, and E. Fretwurst — Universität Hamburg

P-type low gain avalanche diodes are silicon sensors with an intrinsic charge multiplication gain layer. They offer high temporal resolution and are foreseen to be used in HL-LHC timing detectors but are susceptible to radiation damage. Especially in the highly boron doped gain layer the acceptor removal effect occurs, leading to boron defect formation. This process not only deactivates the boron atoms as dopants but also leads to the formation of BiOi defects. These defects are detrimental to the gain layer as they counteract the local electric field by providing positive space charge, eventually removing the gain layer. Carbon co-doping has shown promising results in mitigating gain loss, as the implantation of carbon atoms is believed to influence the boron defect formation kinetically. The study of radiation-induced defects in the gain layer using microscopic defect spectroscopy techniques is challenging as it is difficult to distinguish between bulk and gain layer. To enable more precise investigation of defect kinetics, silicon diodes on highly doped p-type substrates mimicking the gain layer were produced, a total of 25 wafers with test structures covering various doses of carbon implantation, phosphorous co-doping, and oxygenation. This extensive set of samples allows to systematically investigate and thereby parametrize the acceptor removal effect. In this talk the analysis of the samples before and after irradiation including DLTS, TSC and IV/CV measurements is presented.

T 52.6 Wed 17:30 KH 01.012

Characterisation of an Enhanced Lateral Drift (ELAD) Sensor Prototype — •Judith Schlaadt, Naomi Davis, Doris Eckstein, Moritz Guthoff, Simon Spannagel, Anastasiia Velyka, and Gianpiero Vignola — DESY, Hamburg, Germany

The development of vertex and tracking detectors for future lepton colliders faces various challenges regarding time and position resolution while maintaining a low material budget and the capability to process high particle rates. In this context, one approach to improve the spatial resolution is to utilise the effect of charge sharing Here, the ratio of the signal amplitudes measured by neighbouring readout electrodes gives information about the hit position of the traversing particle. By applying a magnetic field and exploiting the Lorentz drift of the generated charge carriers in the sensor volume, charge sharing can be observed. Also, tilting the sensor results in the same effect. However, neither approach is suitable for vertex detectors, since the effect is not sufficient in the case of thin sensors.

The enhanced lateral drift (ELAD) sensor prototype addresses these requirements by featuring a multiple-layer design including buried doping implants. The deep implants generate an additional lateral electric field inside the sensor bulk, resulting in increased charge sharing.

Through simulations, the sensor design was optimised to allow for position-dependent charge sharing close to the theoretical optimum, which results in an improved impact position interpolation. This talk presents first results of the characterisation of an ELAD sensor prototype.

T 52.7 Wed 17:45 KH 01.012

The ATLAS High Granularity Timing Detector: Quality Control Results on Low Gain Avalanche Diodes — •Theodoros Manoussos[1,2], Simon Koch[1], Guilherme Saito[3], Marco Leite[3], Dominik Dannheim[1], Stefan Guindon[1], and Lucia Masetti[2] — [1]CERN — [2]Johannes Gutenberg-Universität Mainz, Germany — [3]Universitade de São Paulo, Brasil

The increase in instantaneous luminosity at the High Luminosity-LHC will be a challenge for the ATLAS detector, as the pile-up is expected to increase to an average of 200 interactions per bunch crossing. To sustain current physics performance and mitigate pile-up effects, a High Granularity Timing Detector (HGTD) will be integrated into the ATLAS end-cap regions, covering a pseudorapidity range of $2.4 \leq |\eta| \leq 4.0$. HGTD aims to achieve 30 ps per-track time resolution for MIPs in the beginning of the lifetime, up to 50 ps after a maximum fluence of $2.5 \cdot 10^{15}$ $\mathrm{n_{eq}/cm^2}$. High-precision timing information improves the correct assignment of tracks to vertices. HGTD sensors are based on the Low Gain Avalanche Diode (LGAD) technology. They provide moderate internal gain, resulting in fast rise time and large signal-to-noise ratio, required for excellent time resolution. Each sensor is a 15×15 array of 1.3×1.3 $\mathrm{mm^2}$ LGAD pads. Along with the sensors, an equal amount of Quality Control-Test Structures (QC-TS) is produced to monitor the quality and uniformity of wafers and extract various technology and fabrication parameters during production. This contribution presents process quality control measurements on QC-TS of the initial phase of the HGTD sensor production.

T 52.8 Wed 18:00 KH 01.012

Module assembly for the ATLAS High Granularity timing detector — •Hendrik Smitmanns[1], Jessica Höfner[1], Frederic Maximilian Matthias Silvan Fischer[1], Annika Stein[1], Lucia Masetti[1], Andrea Brogna[2], Atila Kurt[2], Fabian Piermaier[2], Steffen Schönfelder[2], Quirin Weitzel[2], and Florian Lika[2] — [1]Institut für Physik, Johannes-Gutenberg Universität Mainz — [2]PRISMA+ Detector Lab, Johannes-Gutenberg Universität Mainz

To meet the challenges of the High Luminosity Large Hadron Collider (HL-LHC), especially the increase of pile-up interactions, the ATLAS detector will need to be upgraded. One of the foreseen upgrades will be the installation of the High-Granularity Timing Detector (HGTD). The HGTD will mitigate the effects of pile-up in the ATLAS forward region, providing a time resolution of about $30 - 50$ ps per track. The active detector area consists of 2-double-sided disks per end-cap. A disc side contains about 1000 modules, each consisting of two $2x2$ cm^2 Low Gain Avalanche Detectors which are bump-bonded to two ASICs and glued to a PCB. Multiple modules are then glued onto a support unit to form a detector unit, which will then be built into the final detector at CERN. The current phase of pre-production is used to test and finalize all procedures towards production, for while around 1000 modules, roughly 10 % of the final detector, will be assembled at Johannes Gutenberg University Mainz, one of the six assembly sites. The complete assembly procedure of the final version of the detector module is presented, with focus on assembly, metrology, wire bonding, initial testing and the assembly process for the detector units.