T 6: Electronics, Trigger, DAQ I

Time: Monday 16:15–18:15 Location: KH 00.023

T 6.1 Mon 16:15 KH 00.023

Next-Generation Readout ASIC for DEPFET Pixel Detectors in 65-nm CMOS — •Vasiliki Gogolou, Hans Krüger, and Jochen Dingfelder — University of Bonn, Germany

The continued evolution of particle-physics experiments places increasing demands on the performance, efficiency, and integration density of readout electronics. As detector systems grow in channel count and as data rates accelerate, high-quality, low-noise readout chains become essential to preserve the precision of the underlying sensor technology. DEPFET (Depleted p-channel field effect transistor) pixel sensors play a key role in this landscape with successful applications ranging from high-energy physics vertex detectors such as those for the ILC and Belle II to advanced medical imaging systems. This work presents a next-generation readout integrated circuit for DEPFET matrices, implemented in a state-of-the-art 65-nm CMOS process node. The transition to a smaller feature size enables improved power-area efficiency while maintaining low noise. Each channel integrates a cascode transimpedance amplifier and a compact single-ended-to-differential stage, optimized to fully drive the input range of a high-speed, low-power SAR ADC (successive-approximation register analog-to-digital converter). The readout architecture is specifically designed to interface seamlessly with such ADCs, enabling a system that meets stringent constraints on power density and pixel pitch while delivering the precision required for future high-rate, high-resolution experiments.

T 6.2 Mon 16:30 KH 00.023

Firmware developments and hardware tests for the HL-LHC ATLAS Liquid Argon Signal Processor system — Peter Fischer, •Markus Helbig, Rainer Hentges, Arno Straessner, Johann C. Voigt, and Philipp Welle — Institut für Kern- und Teilchenphysik, TU Dresden

In the HL-LHC era, the ATLAS Liquid Argon Calorimeters will be equipped with the new LAr Signal Processors (LASP). This off-detector processing system based on Altera Agilex 7 FPGAs will perform energy reconstruction for all 182 468 detector cells at every bunch crossing in real time and provide them to the new trigger systems Global Event Processor (GEP) and the Forward Feature Extractor (fFEX) as well as the main readout.

To cope with the higher pile-up, the use of 1-dimensional Convolutional Neural Networks (CNNs) with up to 400 parameters for energy reconstruction has been studied as an alternative to the current Optimal Filter approach. Using efficient FPGA resource allocations, a sufficient number of CNN instances to process up to 384 cells are fit on a single FPGA, leaving enough resources for other components. Their implementation has been verified in standalone hardware setups based on FPGA development kits and LASP testboards.

Furthermore, the first Agilex-based prototype board has recently become available. On this board, the interfaces from the front-end and towards the trigger systems are implemented as optical transceivers using Samtec FireFly modules. Their performance is studied to guarantee reliable data transmission.

T 6.3 Mon 16:45 KH 00.023

The ATLAS Tile Calorimeter Trigger and Data Acquisition Interface: Final Design Overview and Validation Results — •Maximilian Köper and Thomas Junkermann — Kirchhoff-Institut für Physik, Heidelberg University

The ATLAS experiment is undergoing the Phase-II Upgrade to accommodate the High Luminosity LHC (HL-LHC), necessitating a complete redesign of the trigger and readout architectures to handle increased pile-up. This contribution focuses on the Tile Calorimeter's Trigger and Data Acquisition interface (TDAQi), an ATCA Rear Transition Module designed to bridge the off-detector electronics with the ATLAS Level-0 trigger systems.

Equipped with an AMD Kintex UltraScale+ FPGA, the TDAQi receives calibrated cell energies and computes trigger primitives at 40 MHz. Key processing tasks include forming coarse-granularity objects for electron/jet triggers, identifying muon hits, and sorting high-energy cells for the Global Trigger Processor. These operations must be executed within a strict 250 ns latency budget while managing high-speed links up to 11.2 Gbps.

We present the TDAQi design and its role in the real-time data path. The discussion focuses on the final hardware validation and integration tests required before the start of the in-house production phase. We report on the performance of the latest pre-production modules, which serve as the final verification step for the upcoming series assembly.

T 6.4 Mon 17:00 KH 00.023

Electron algorithm studies for the ATLAS forward Feature Extractor — •Florian Harz, Hannes Mildner, and Stefan Tapprogge — Institut für Physik, JGU, Mainz, Germany

The High-Luminosity LHC upgrade presents unprecedented challenges for real-time event selection in the ATLAS experiment, driven by significantly increased rates, pile-up conditions, and the need for fast, high-precision triggering. The forward Feature Extractor (fFEX) board, based on high-performance FPGAs, will play a central role in the Level-0 calorimeter trigger, enabling low-latency identification of electromagnetic signatures in the forward area. This presentation summarizes recent algorithmic studies performed for the fFEX electron identification pipeline, highlighting strategies that balance physics performance with the stringent timing and resource constraints inherent to FPGA-based processing. A sliding-window algorithm has been implemented in firmware to act as a baseline comparison as it has been used previously used in ATLAS calorimeter triggering. Building on this, the use of machine-learning approaches is explored with the goal to have a full implementation in firmware that surpasses the legacy sliding-window method.

T 6.5 Mon 17:15 KH 00.023

Development of the clustering algorithm for the LHCb Upgrade II SciFi tracker — •Jan Sorokovski, Michael Lupberger, and Marco Gersabeck — Albert-Ludwigs-Universität Freiburg, Freiburg im Breisgau, Germany

The LHCb Upgrade II aims to increase the instantaneous luminosity by a factor of 5. To achieve that, many detector systems have to be upgraded to address the increased detector occupancy and pileup. This includes the new downstream tracker, the Mighty Tracker, which will combine silicon pixel sensors in the high-occupancy region and improved Scintillating Fibres (SciFi) in the remaining region.

One of the key challenges of the SciFi Tracker is the handling of the output of the advanced front-end chip. For that, the development of an efficient, real-time clustering algorithm capable of processing the increased data volume, while maintaining a high spatial resolution and track hit efficiency, is crucial. A major consideration are noise sources, which have to be identified, understood and characterised to provide robustness against noise and to improve overall performance.

In this presentation, an early algorithm design and noise considerations and studies are

T 6.6 Mon 17:30 KH 00.023

Full Path Data Injection for an FPGA-Based Data Acquisition System — •Bent Buttwill for the Mu3e-Collaboration — Institut für Kernphysik, Johannes Gutenberg-Universität Mainz

The Mu3e experiment, located at the Paul Scherer Institute in Switzerland, aims to study the charged-lepton-flavour violating decay $\mu^+ \to e^+e^+e^-$. To achieve the goal of probing the branching fraction beyond 10^{-15} in Phase I, the experiment is designed to detect 10^8 muon decays per second.

The FPGA-based data acquisition system for Mu3e is designed to handle a data production rate of approximately 100 Gbit/s. Its hardware is optimized for efficient resource utilization and sustained high-throughput operation. Continuous verification of the data pipeline during development is essential to ensure reliable and performant operation.

Previously, test data was injected into internal memory locations within the FPGA, limiting the scope of the test procedure to a subset of the full pipeline. This work investigates a new data injection approach that enables testing of the complete pipeline. In this approach, data is injected digitally at the optical input interface of the FPGA, allowing the test data to propagate through the entire design, therefore testing every component of the firmware.

T 6.7 Mon 17:45 KH 00.023

Investigation of Electronic Crosstalk in the Optical Mod-

ules of the Pacific Ocean Neutrino Experiment — •Lars von der Werth for the P-ONE-Collaboration — Technische Universität München

The Pacific Ocean Neutrino Experiment (P-ONE) is a proposed cubic-kilometer*scale neutrino detector to be deployed in the Pacific Ocean. Its fundamental detection units are the P-ONE optical modules (P-OMs), each housing 16 photomultiplier tubes (PMTs) to record Cherenkov light emitted by secondary particles produced in high-energy neutrino interactions. Each P-OM includes a trigger system that performs an initial selection of relevant signals. A detailed understanding of the internal electronic crosstalk is essential for reliable triggering. To characterize these effects, electromagnetic interference (EMI) measurements help identify the dominant noise sources and investigate the pathways through which these couple into the PMT signal. Further, we present how different grounding schemes, cabling configurations, and shielding strategies affect the crosstalk level observed in the different PMT positions within the P-OM.

T 6.8 Mon 18:00 KH 00.023

Emulator-Based Evaluation of FPGA Algorithms for the ATLAS MDT Trigger Processor — •Marcel Marques Boonen, Davide Cieri, Oliver Kortner, and Sandra Kortner — Max Planck Institute for Physics , Garching, Germany

The Monitored Drift Tube Trigger Processor (MDTTP), a new FPGA-based component of the High- Luminosity LHC upgrade of the ATLAS muon trigger, is being developed to reconstruct muon tracks at the first-level trigger using the information from the MDT detectors. Two proposals for the determination of the muon transverse momenta are currently under investigation: an algorithm that translates the sagitta of the muon trajectory into transverse momentum using pre-defined conversion functions, and a machine-learning approach that exploits the directions and positions of the muon trajectory in the muon chambers.

Both approaches rely on a data processing chain capable of buffering and handling large data streams. To simulate such data processing under realistic conditions, dedicated Monte Carlo data are stored in DDR memories of one MDTTP board and then sequentially injected via optical fibers into the MDTTP board under test. This presentation will describe the implementation of this approach and its application in evaluating the performance of the aforementioned transverse-momentum calculation procedures.